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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,838	UEDA, NAOHIRO	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/14/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 12, 2008 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-4 and 17** are rejected under 35 U.S.C. 103(a) as being obvious over **Takasu et al. (US 6,369,409;** previously cited, hereinafter, Takasu) in view of **Zuniga et al. (US 2002/0000671**; previously cited, hereinafter, Zuniga).

With respect to **claim 1, Takasu** teaches a semiconductor apparatus **(FIG. 12A-12F)** comprising:

a semiconductor substrate **(801; FIG. 12A, col. 8: lns. 9-10)**;

an electrode pad **(814, col. 9: lns. 44-58)** comprising a metal layer **("aluminum," col. 9: ln. 44)** and formed over the semiconductor substrate **(801, FIG.**

12E), said electrode pad providing contact between said semiconductor apparatus and external circuitry **(FIGs. 9 and 10) (col. 9: lns. 44-52; it is implicit that the aluminum "wiring" provides contact between an integrated circuit and external circuitry)**;

a MOS transistor **("N-type transistor")** formed over the semiconductor substrate **(col. 9: lns. 23-28)**; and

a circuit **(FIGs. 9, 10 and 12F)** formed over said semiconductor substrate **(801)** in a region under the electrode pad **(814)**, said circuit comprising an array of adjacent resistive elements **(807; FIG. 12D)** formed of a semiconductor material **("polysilicon") (col. 9: lns. 28-67)**.

Thus, Takasu teaches all the limitations of the claim with the exception of explicitly disclosing wherein said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array.

However, **Zuniga** discloses an analogous semiconductor apparatus wherein an electrode pad **(514/515, Figs. 5 and 6)** is formed over an array of resistive elements **(passive resistors)** such that said electrode pad **(514/515)** extends transversely across said array **(¶ [0052], Figs. 5 and 6)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to form the electrode pad over Takasu's array of resistive elements, as taught by Zuniga, for the disclosed intended purpose of saving chip space **(¶ [0049])** and protecting the underlying circuit components **(¶ [0053])**.

With respect to **claim 2, Takasu** teaches wherein the resistive elements **(807)** comprise polysilicon **(col. 9: lns. 28-30)**.

With respect to **claim 3, Takasu** teaches wherein the resistive elements **(807)** include a plurality of resistors connected serially **(807; FIGs. 12D-12F) (col. 9: lns. 28-33, 56-58)**.

With respect to **claim 4, Takasu** teaches wherein the MOS transistor comprises a gate electrode **(806; FIG. 12D)** which comprises polysilicon **(col. 9: lns. 10-15)**.

With respect to **claim 17, Takasu** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the resistive elements includes a plurality of doped semiconductor material resistors **(807; FIG. 12D) (col. 9: lns. 10-33)**.

3. **Claims 1-6, 17, 19 and 20** are rejected under 35 U.S.C. 103(a) as being obvious over **Takasu et al. (US 2002/0145177**; newly cited, hereinafter, Takasu**)** in view of **Zuniga et al. (US 2002/0000671**; previously cited, hereinafter, Zuniga**)**.

With respect to **claim 1, Takasu** teaches a semiconductor apparatus **(FIG. 1)** comprising:

a semiconductor substrate **(101, ¶ [0044])**;

an electrode pad **(¶ [0062]: "aluminum film" 105 connected to regions 401 and arranged to cover region 402)** comprising a metal layer and formed over the semiconductor substrate **(101)**, said electrode pad providing contact between said semiconductor apparatus and external circuitry **(¶ [0063]: it is implicit that the aluminum film 105 provides contact between the integrated circuit and external circuitry)**;

a MOS transistor **(210, ¶ [0044])** formed over the semiconductor substrate **(101)**;

a circuit **(¶ [0063]: "bleeder resistance circuit")** formed over said semiconductor substrate **(101)** in a region under the electrode pad **(105)**, said circuit comprising an array of adjacent resistive elements **(¶ [0061]: "plurality of resistors")** formed of a semiconductor material **(¶ [0061]: "silicon")**.

Thus, Takasu teaches all the limitations of the claim with the exception of explicitly disclosing wherein said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array.

However, **Zuniga** discloses an analogous semiconductor apparatus wherein an electrode pad **(514/515, Figs. 5 and 6)** is formed over an array of resistive elements **(passive resistors)** such that said electrode pad **(514/515)** extends transversely across said array **(¶ [0052], Figs. 5 and 6)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to form the electrode pad over Takasu's array of resistive elements, as taught by Zuniga, for the disclosed intended purpose of saving chip space **(¶ [0049])** and protecting the underlying circuit components **(¶ [0053])**.

With respect to **claim 2, Takasu** teaches wherein the resistive elements **(410)** comprise silicon **(¶ [0061])**. Note, regarding the limitation of "polysilicon," such a material for thin film resistors is well known and conventional **(¶ [0064])**, and thus would have been obvious to one of ordinary skill in the art at the time of the invention.

With respect to **claim 3, Takasu** teaches wherein the resistive elements **(410)** include a plurality of resistors connected serially **(¶ [0061])**.

With respect to **claim 4, Takasu** teaches wherein the MOS transistor **(210)** comprises a gate electrode **(205)** which comprises polysilicon **(¶ [0053])**.

With respect to **claim 5, Takasu** teaches wherein the semiconductor apparatus further comprises:

an insulating film **(102, ¶ [0069])** formed on the semiconductor substrate **(101)** in a region in a vicinity of the electrode pad **(105, FIG. 1)**; and

a fuse element **(501, ¶ [0069])** formed on the insulating film **(102, FIG. 1)**, said fuse element in electrical contact with said plurality of resistive elements **(¶ [0071])**.

With respect to **claim 6, Rodriguez** teaches the semiconductor apparatus as set forth in claims 1 and 5 above, wherein the fuse element **(501)** comprises silicon **(¶ [0069])**. Note, regarding the limitation of "polysilicon," such a material for a fuse element is well known and conventional, and thus would have been obvious to one of ordinary skill in the art at the time of the invention.

With respect to **claim 17, Takasu** teaches the semiconductor apparatus as set forth in claim 1 above, wherein the resistive elements **(410)** includes a plurality of doped semiconductor material resistors **(¶ [0061])**.

With respect to **claim 19, Takasu** teaches a semiconductor apparatus **(FIG. 1)** comprising:

a semiconductor substrate **(101, ¶ [0044])**;

an oxide film **(102, ¶ [0044])** formed over the semiconductor substrate **(101)**, the oxide film comprising a resistive-element formation region **(410, ¶ [0060])**, a fuse

element formation region **(510, ¶ [0068])**, and a MOS transistor forming region **(210, ¶ [0044])**, the resistive element forming region **(410)** having a circuit comprising an array of strip-shaped resistive elements **(¶ [0061], FIG. 1)** formed of a semiconductor material **(¶ [0061]: "silicon")**;

an insulating layer **(104, ¶ [0062])** formed over the oxide film **(102, FIG. 1)** and having an electrode-pad formation region **(105)**,

wherein the electrode-pad formation region **(105, ¶ [0062])** is formed over the resistive-element formation region **(410, FIG. 1)**, and wherein the electrode-pad formation region has an electrode pad comprising a metal layer **(¶ [0062]: "aluminum")**.

Thus, Takasu discloses all the limitations of the claim with the exception of explicitly disclosing wherein the electrode pad extends transversely across the array of strip-shaped resistive elements. However, **Zuniga** discloses an analogous semiconductor apparatus wherein an electrode pad **(514/515, Figs. 5 and 6)** is formed over an array of resistive elements **(passive resistors)** such that said electrode pad **(514/515)** extends transversely across said array **(¶ [0052], Figs. 5 and 6)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to form the electrode pad over Takasu's array of strip-shaped resistive elements, as taught by Zuniga, for the disclosed intended purpose of saving chip space **(¶ [0049])** and protecting the underlying circuit components **(¶ [0053])**.

With respect to **claim 20, Takasu** teaches wherein a respective low-resistance silicon region **(401, FIG. 1)** is formed immediately next to the lengthwise ends of each of

the plurality of resistive elements **(¶ [0061])**. Note, regarding the limitation of "polysilicon," such a material for thin film resistors is well known and conventional **(¶ [0064])**, and thus would have been obvious to one of ordinary skill in the art at the time of the invention.

4. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Takasu ('177; cited above) and Zuniga ('671; cited above)** as applied to claim 5 above, and further in view of **Matsuzaki et al. (US 2002/0063262, previously cited, hereinafter, Matsuzaki)**.

With respect to **claim 7, Takasu and Zuniga** teach all the limitations of the claim, as set forth above in claim 1, with the exception of disclosing:

a rerouting layer formed in a region above the fuse element; and

an external connection terminal formed on the rerouting layer in a region different from a formation region of the electrode pad.

However, **Matsuzaki** teaches a semiconductor apparatus **(FIG. 3)** wherein a rerouting layer **(148)** is formed in a region above a fuse element **(142; pg. 5: [0093])**; and an external connection terminal **(150)** is formed on the rerouting layer in a region different from a formation region of the electrode pad **(143) (pg. 4: [0080]-[0081])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Matsuzaki, into the semiconductor apparatus of Takasu and Zuniga, for the disclosed intended purpose of connecting the

semiconductor apparatus to an electrode of another chip, thereby forming a multi-chip apparatus **(pg. 4: [0082])**.

5. **Claims 8-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takasu ('177; cited above) and Zuniga ('671; cited above)** as applied to claim 5 above, and further in view of **Tsuchida (US 6,232,823, previously cited)**.

With respect to **claim 8, Takasu and Zuniga** teach the semiconductor apparatus as set forth in claim 5 above, with the exception of disclosing:

wherein the circuit comprises a voltage setting circuit, the resistive elements comprise at least two resistors for producing a split voltage based on an input source power voltage, and the voltage setting circuit changes the split voltage according to a condition of the fuse element.

However, **Tsuchida** teaches voltage setting circuit **(fig. 1)**, in which a resistive elements comprise at least two resistors **(22, 23, 24, 25, 26)** for producing a split voltage based on an input source power voltage **(21)**, and the voltage setting circuit changes the split voltage according to a condition of the fuse element **(27, 28, 29, 30) (col. 7: lns. 7-64)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Tsuchida, into the semiconductor apparatus of Takasu and Zuniga, for the disclosed intended purpose of providing a voltage setting circuit, in which the number of choices in the output voltage is increased while suppressing the increase of an area occupied by resistors **(col. 2, lns. 24-27)**.

With respect to **claim 9, Tsuchida** teaches **(fig. 6)** wherein the resistive elements comprise at least two resistors **(22, 23, 24, 25, 26)** for producing a split voltage **(col. 11: lns. 51-55; col. 7: 45-64)** based on an input source power voltage **(53)**, the circuit comprises a reference voltage generator **(51)** for generating a reference voltage **(col. 11: lns. 61-63)** and a voltage detector including a comparator **(52)** for performing a comparison of the split voltage with the reference voltage **(col. 11: lns. 50-67; col. 12, lns. 1-33)**. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Tsuchida, into the semiconductor device of Takasu and Zuniga, for the reasons stated above in claim 8.

With respect to **claim 10, Tsuchida** further teaches **(fig. 6)** wherein the apparatus further comprises an output driver **(54)** for controlling an output voltage **(55)** based on an input voltage **(53)**, and the comparator **(52)** of the voltage detector outputs a gate control voltage **("operation voltage")** as a result of the comparison for controlling the output driver **(54)** to control the output voltage **(col. 11, lns. 61-67; col. 12, lns. 1-5)**. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Tsuchida, into the semiconductor apparatus of Takasu and Zuniga, for the reasons stated above in claim 8.

6. **Claims 18 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takasu ('177; cited above) and Zuniga ('671; cited above)** as applied to claims 4 and 19, respectively, and further in view of **Kohda et al. (US 5,107,313, previously cited, hereinafter, Kohda)**.

With respect to **claims 18 and 21, Takasu** further teaches wherein the MOS transistor formation region **(210, FIG. 1)** includes a MOS transistor comprising a gate electrode **(205)** formed of a material comprising polysilicon **(¶ [0053])**. Thus, Takasu and Zuniga disclose all the limitations of the claims as set forth above, with the exception of disclosing wherein the gate electrode has lengthwise ends which are bent in an upward direction over the oxide film.

However, **Khoda** teaches a semiconductor apparatus wherein the gate electrode **(4b)** has lengthwise ends which are bent in an upward direction over an oxide film **(2) (FIG. 10; col. 6, lns. 6-12)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Khoda, into the semiconductor apparatus of Takasu and Zuniga, to form the gate electrode with lengthwise ends bent in upward direction over an oxide film, for the disclosed intended purpose of reducing the horizontal spacing between the gates, which thereby reduces the cell area and leads to a higher cell density of memory devices **(col. 6: lns. 21-24)**.

Response to Arguments

7. Applicant's arguments filed June 12, 2008, have been fully considered but are moot in view of new grounds of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814